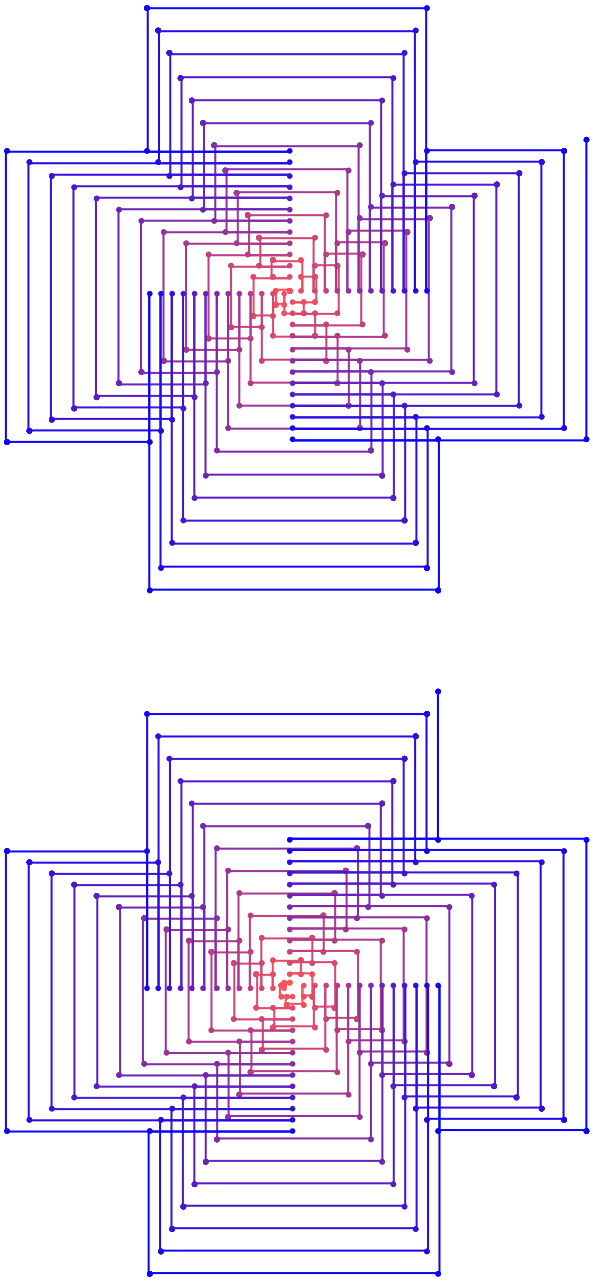
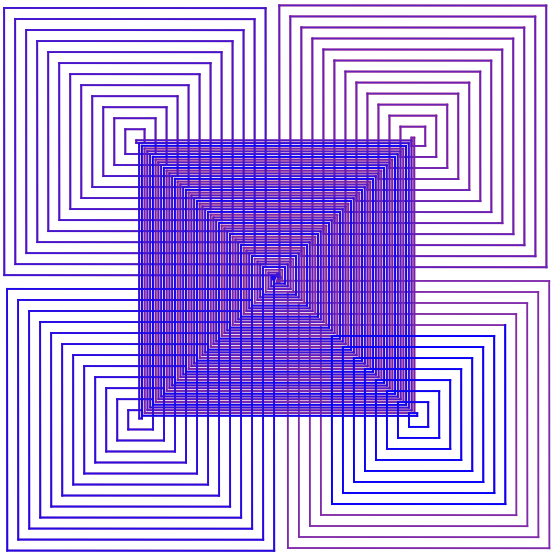
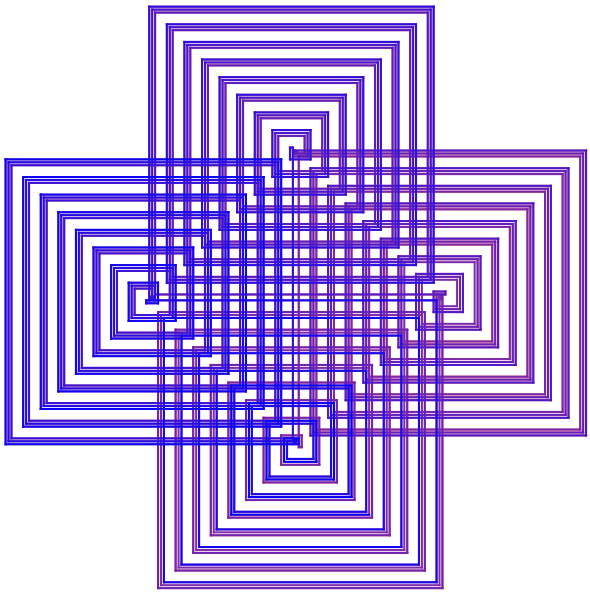
Unit 3 ⟹ February 2018 harvest

AsSis aided design of hypothetical EMGeng integrated circuits

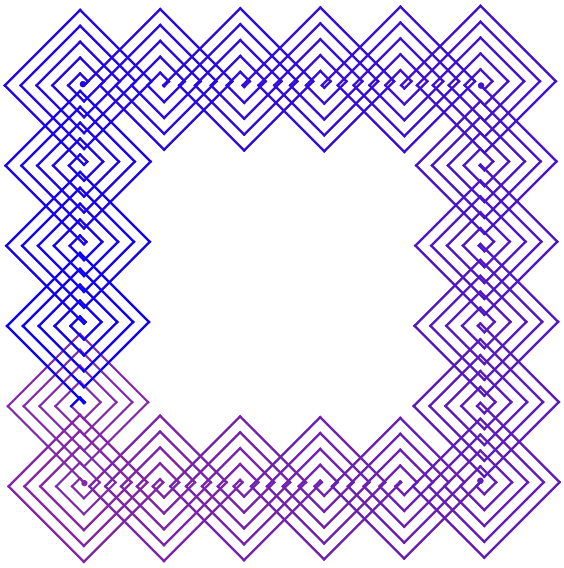


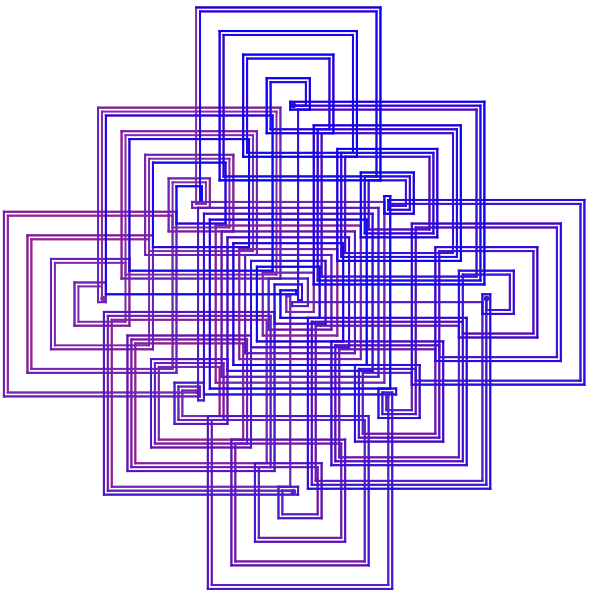
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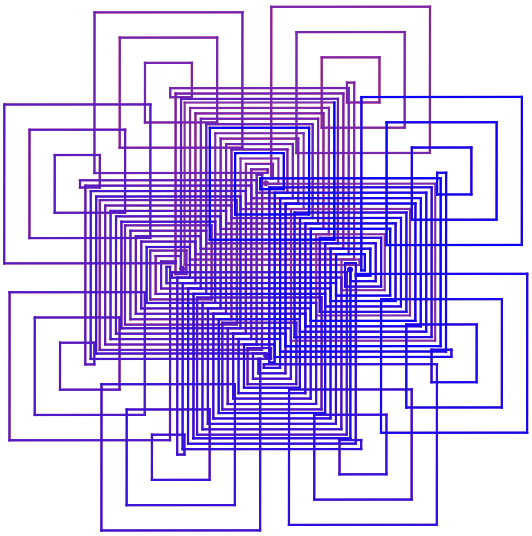


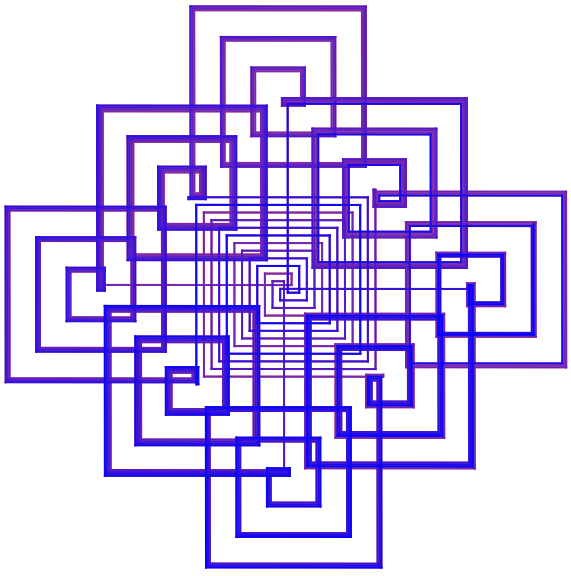
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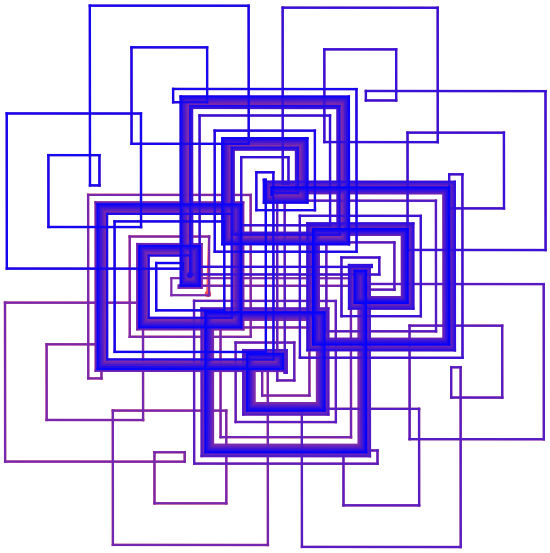


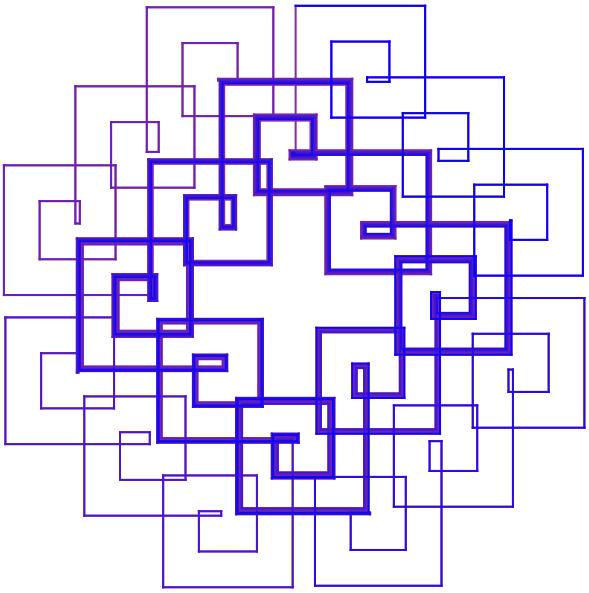
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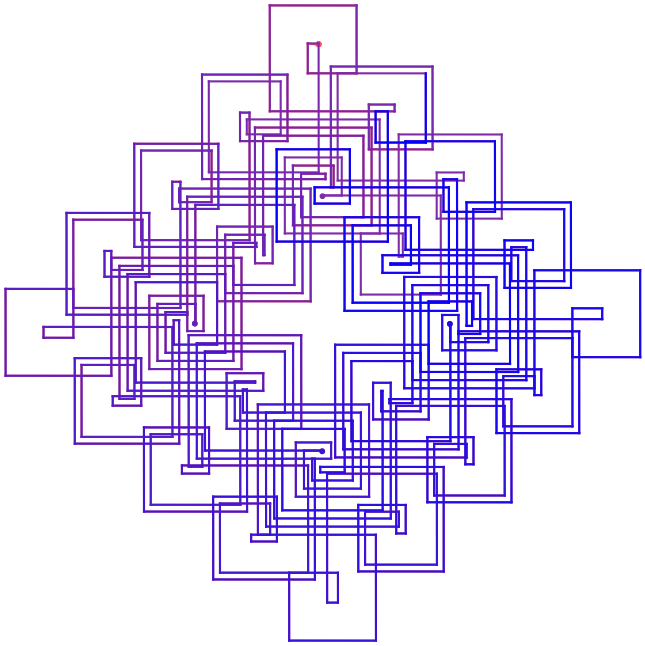


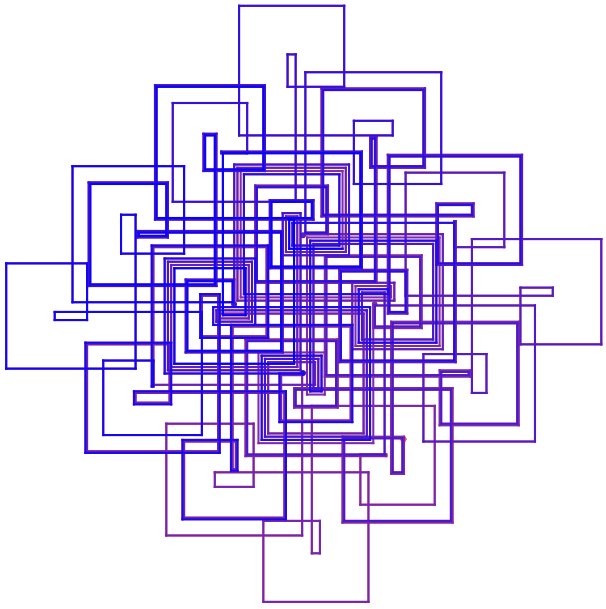
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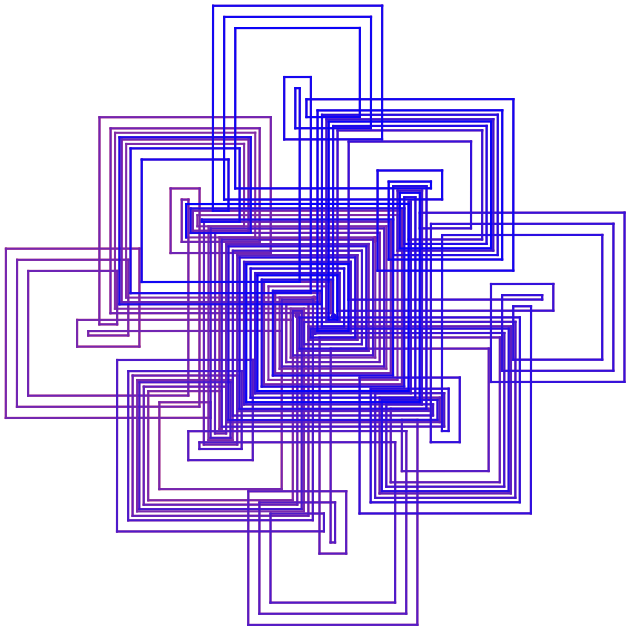


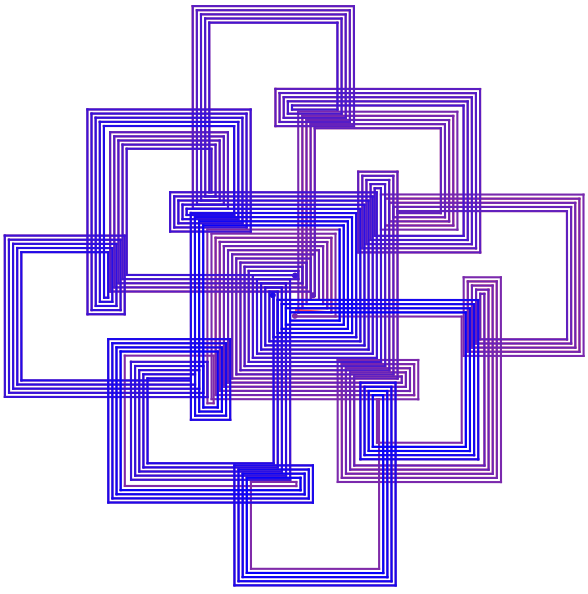
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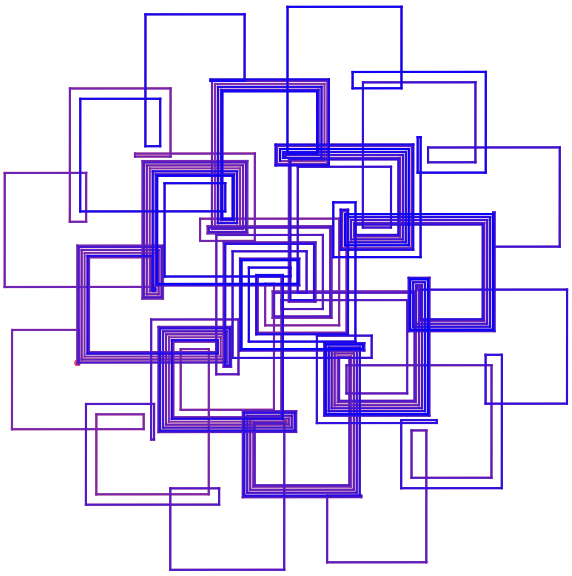


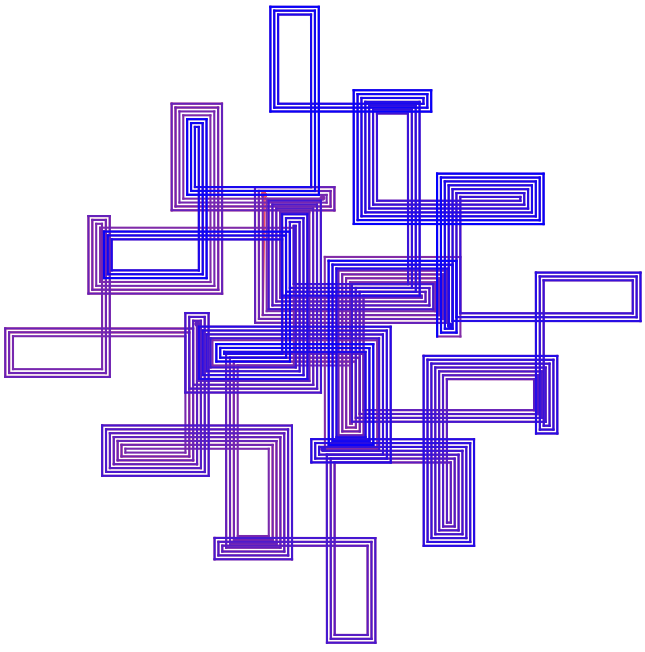
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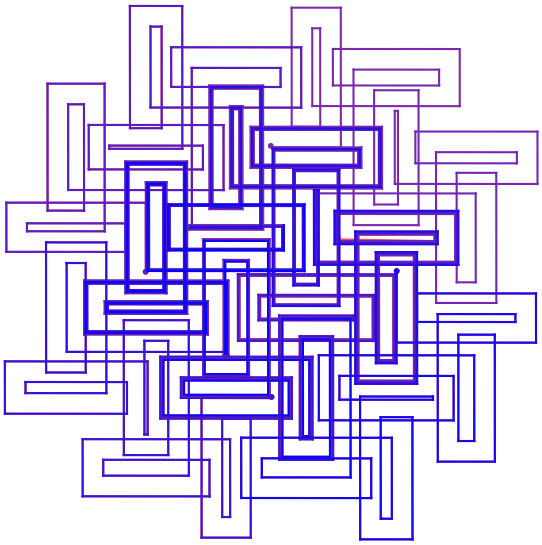


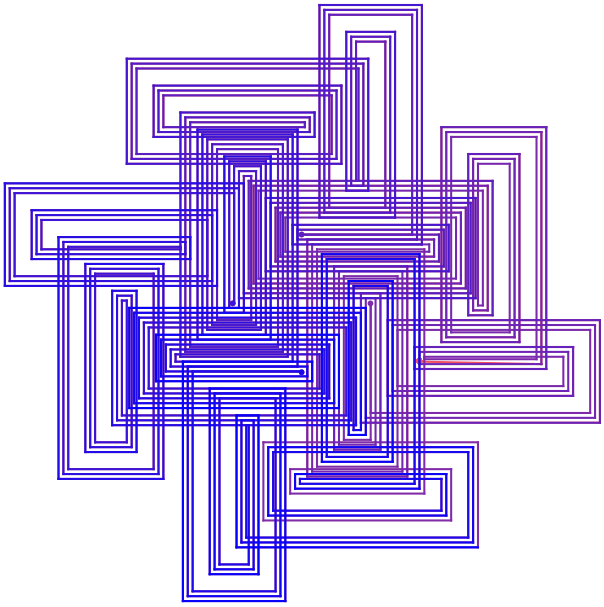
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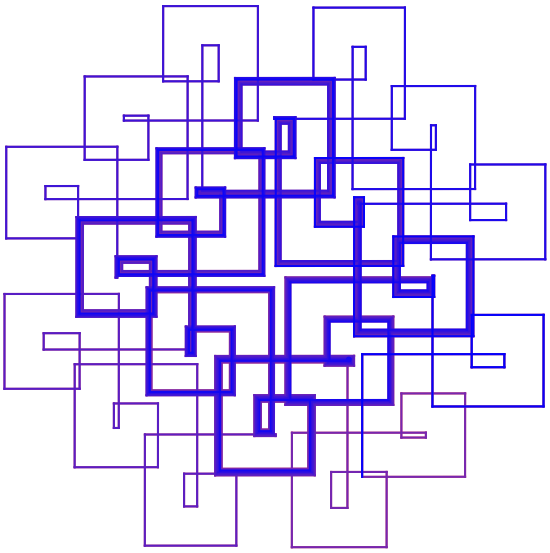


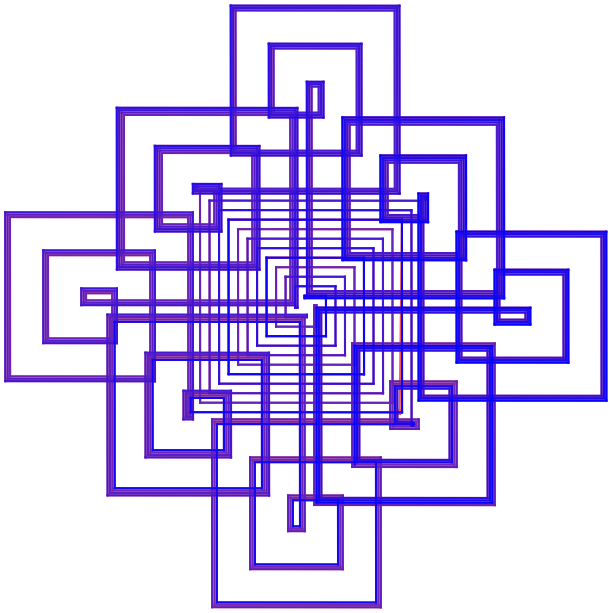
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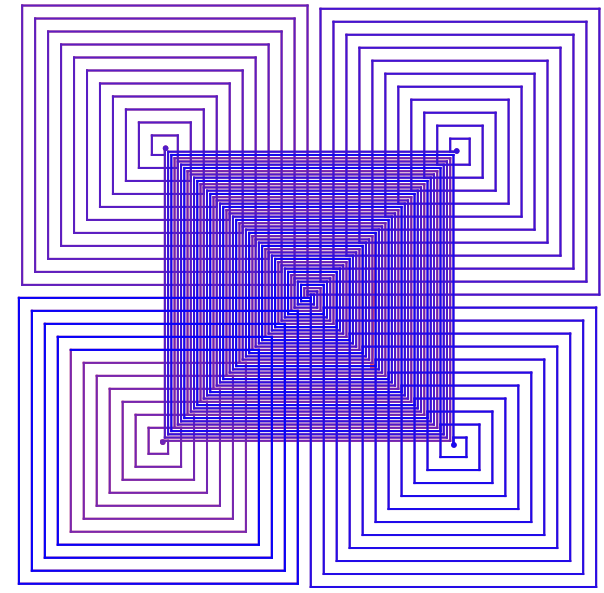


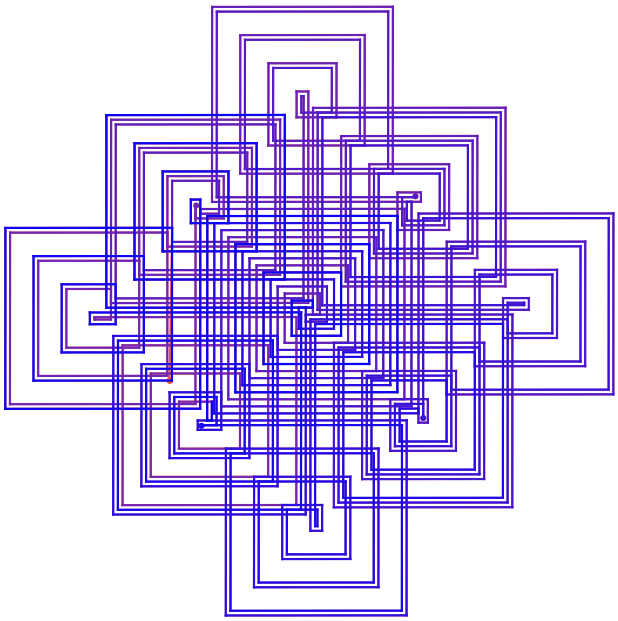
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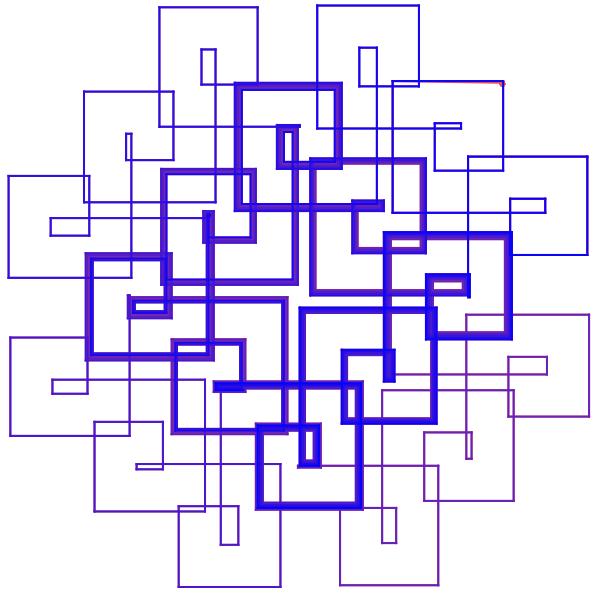


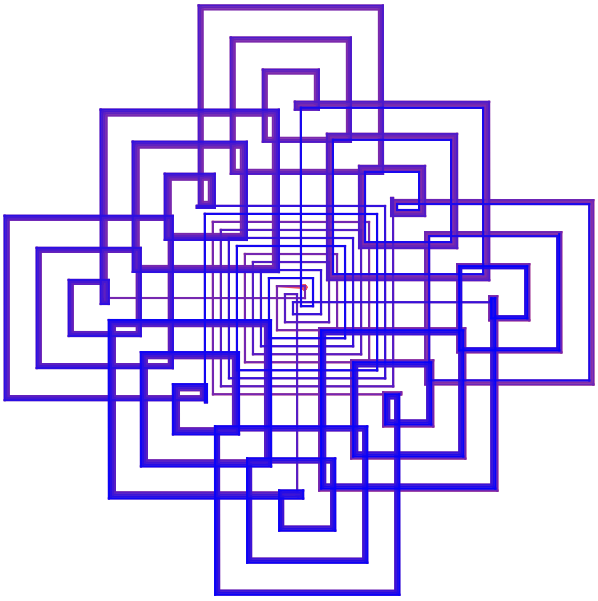
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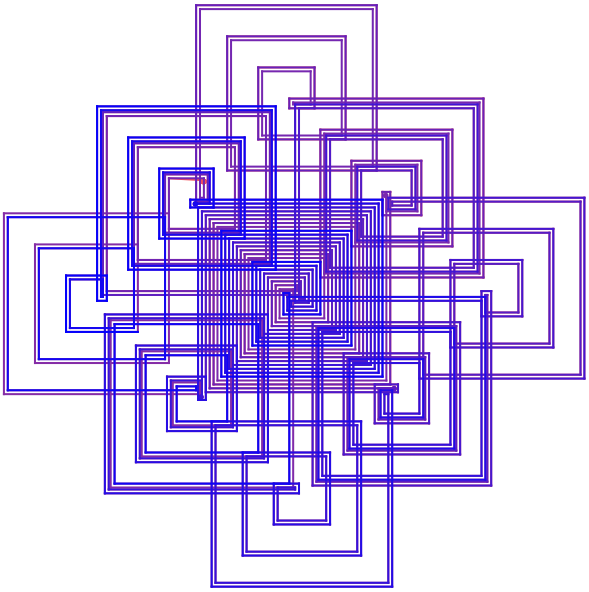


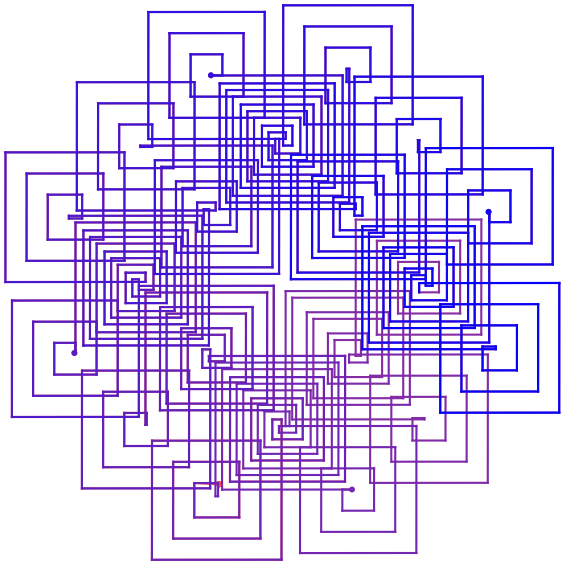
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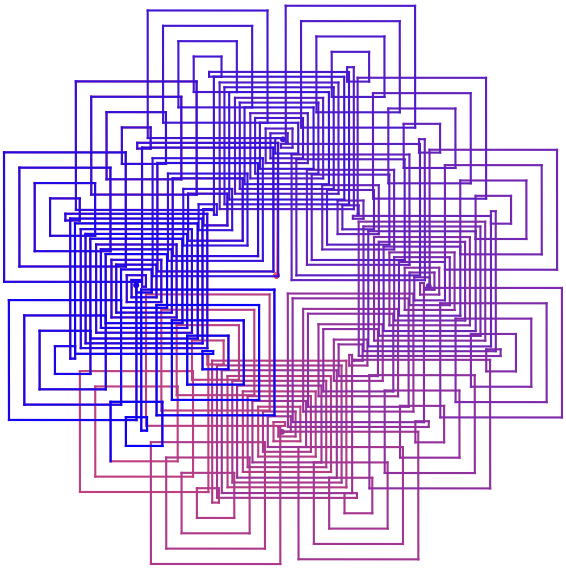


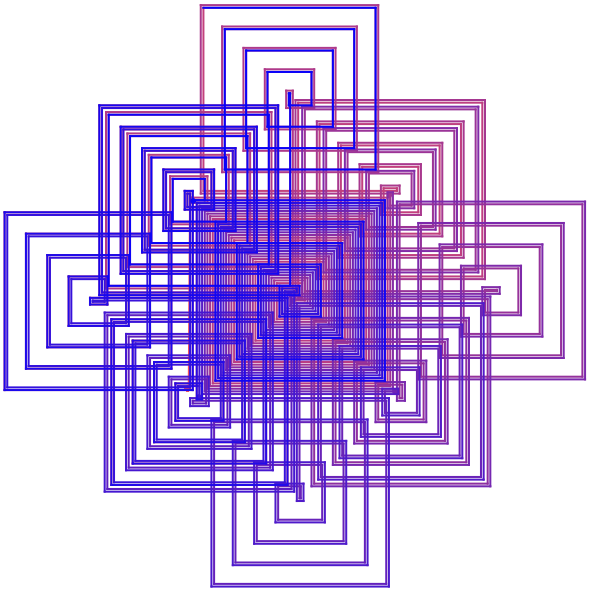
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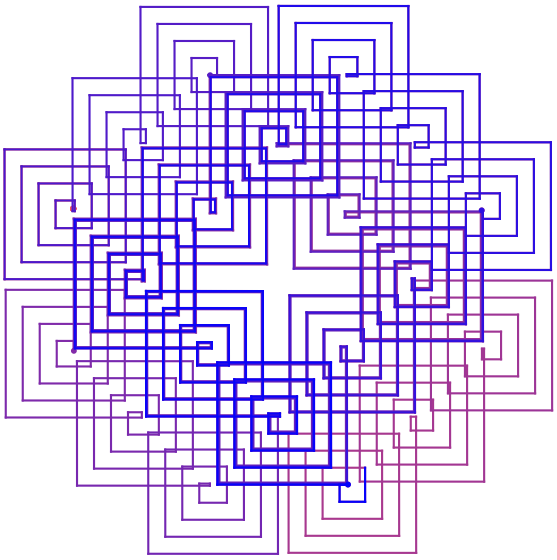


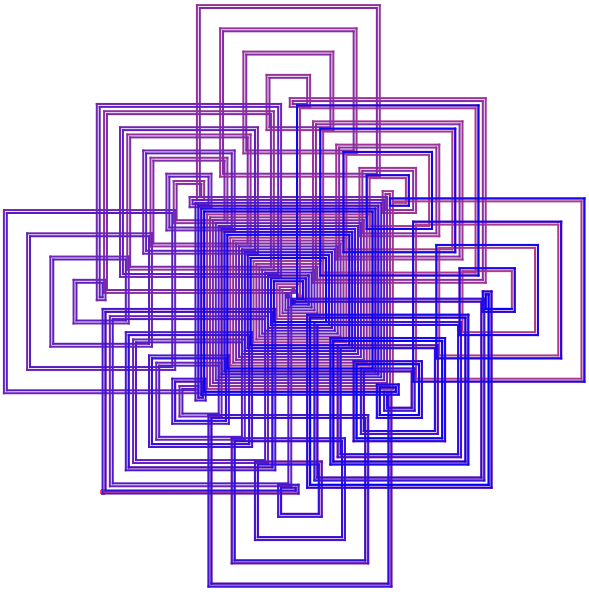
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